Si5023-EVB

EVALUATION BOARD FOR Si5023 SiPHY™ MULTI-RATE SONET/SDH CLOCK AND DATA RECOVERY IC

Description

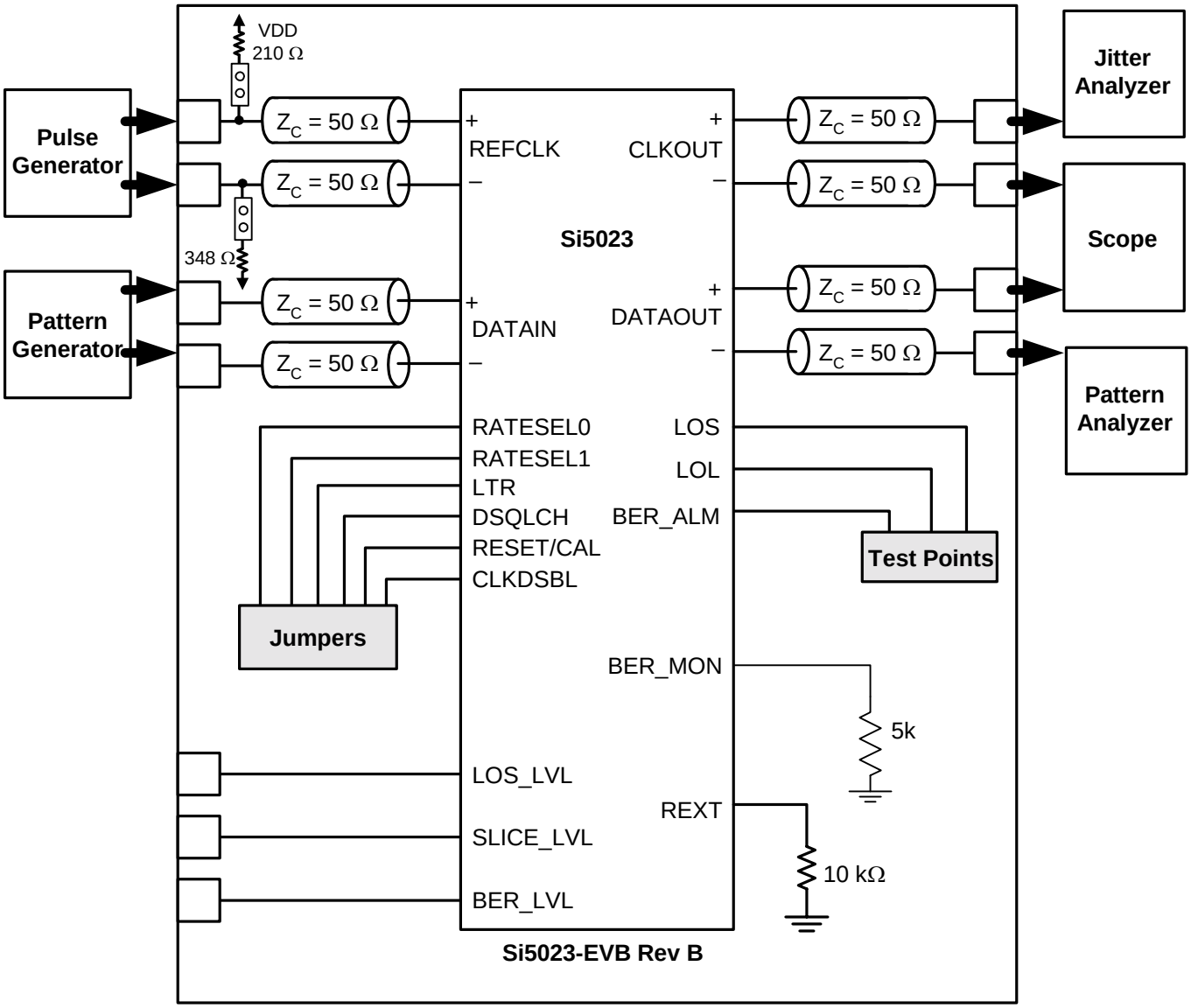
The Si5023 evaluation board provides a platform for testing and characterizing Silicon Laboratories' Si5023 SiPHY™ multi-rate SONET/SDH clock and data recovery IC. The Si5023 CDR supports OC-48/12/3, STM-16/4/1, Gigabit Ethernet, and 2.7 Gbps FEC rates.

All high-speed I/Os are ac coupled to ease interfacing to industry standard test equipment.

Features

- Single 3.3 V power supply
- Differential I/Os ac coupled
- Simple jumper configuration

Functional Block Diagram



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Functional Description

The evaluation board simplifies characterization of the Si5023 Clock and Data Recovery (CDR) device by providing access to all of the Si5023 I/Os. Device performance can be evaluated by following the "Test Configuration" section. Specific performance metrics include input sensitivity, jitter tolerance, jitter generation, and jitter transfer.

Power Supply

The evaluation board requires one 3.3 V supply. Supply filtering is placed on the board to filter typical system noise components; however, initial performance testing should use a linear supply capable of supplying the nominal voltage ±5% dc.

CAUTION: The evaluation board is designed so that the body of the SMA jacks and GND are shorted. Care must be taken when powering the PCB at potentials other than GND at 0.0 V and VDD at 3.3 V relative to chassis GND.

Device Powerdown

The CDR can be powered down via the RESET/CAL signal. When asserted, the evaluation board will draw minimal current. RESET/CAL is controlled via one jumper located in the lower left-hand corner of the evaluation board. RESET/CAL is wired to the signal post adjacent to the VDD post. For a valid reset to occur when using external reference clock mode, a proper external reference clock frequency must be applied as specified in Table 1. CLKOUT, DATAOUT, DATAIN CLKOUT, DATAOUT, and DATAIN (all high-speed I/Os) are wired to the board perimeter on 30 mil (0.030 inch) 50 Ω microstrip lines to the end-launch SMA jacks as labeled on the PCB. These I/Os are ac coupled to simplify direct connection to a wide array of standard test hardware. Because each of these signals are differential, both the positive (+) and negative (–) terminals must be terminated to 50 Ω. Terminating only one side will adversely degrade the performance of the CDR. The inputs are terminated on the die with 50 Ω resistors.

Note: The 50 Ω termination is for each terminal/side of a differential signal, thus the differential termination is actually 50 Ω + 50 Ω = 100 Ω.

REFCLK

REFCLK is optional for clock and data recovery within the Si5023 device. If REFCLK is not used, jumper both JP15 and JP16. These jumpers pull the REFCLK+ input to VDD and REFCLK– input to GND, which configures the device to operate without an external reference.

When applied, REFCLK is used to center the frequency of the DSPLL™ so that the device can lock to the data. Ideally, the REFCLK frequency should be 1/128th, 1/32nd, or 1/16th the VCO frequency and must have a frequency accuracy of ±100 ppm. Internally, the CDR automatically recognizes the REFCLK frequency within one of these three frequency ranges. Typical REFCLK frequencies are given in Table 1. REFCLK is ac coupled to the SMA jacks located on the top side of the evaluation board.

Table 1. Typical REFCLK Frequencies

SONET/SDH	Gigabit Ethernet	SONET/SDH with 15/14 FEC	Ratio of VCO to REFCLK
19.44 MHz	19.53 MHz	20.83 MHz	128
77.76 MHz	78.125 MHz	83.31 MHz	32
155.52 MHz	156.25 MHz	166.63 MHz	16

RATESEL

RATESEL is used to configure the CDR to recover clock and data at different data rates. RATESEL is a two bit binary input controlled via two jumpers located in the lower left-hand corner of the evaluation board. RATESEL0/1 are wired to the center posts (signal post) between VDD and GND. For example, the OC-48 data rate is selected by jumping RATESEL0 to 1 and RATESEL1 to 1.

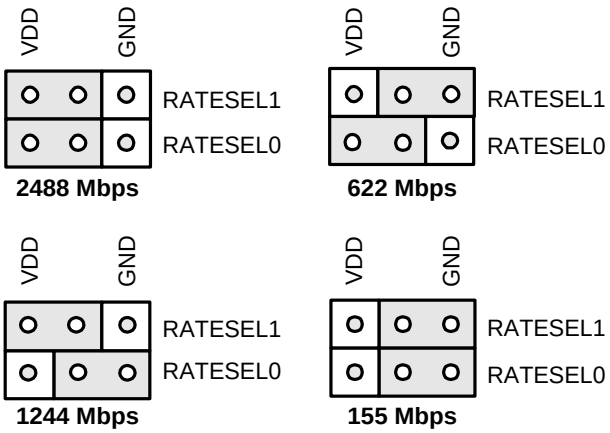


Figure 1. RATESEL Jumper Configurations

Loss-of-Lock (LOL)

Loss-of-lock (LOL) is an indicator of the relative frequency between the data and the REFCLK. LOL will assert when the frequency difference is greater than ±600 ppm. In order to prevent LOL from de-asserting

prematurely, there is hysterisis in returning from the out-of-lock condition. LOL will be de-asserted when the frequency difference is less than ±300 ppm.

LOL is wired to a test point which is located on the upper right-hand side of the evaluation board.

Loss-of-Signal Alarm Threshold Control

The loss-of-signal alarm (LOS) is used to signal low incoming data amplitude levels. The input signal to the threshold control is set by applying a dc voltage level to the LOS_LVL pin. LOS_LVL is controllable through the BNC jack J10. The mapping of the LOS_LVL voltage to input signal alarm threshold level is shown in Figure 2.

The $\overline{\text{LOS}}$ Threshold to $\overline{\text{LOS}}$ Level is mapped as follows:

$$V_{LOS} = \frac{V_{LOS_LVL} - 1.5}{25}$$

If this function is not used, install jumper to JP1 header.

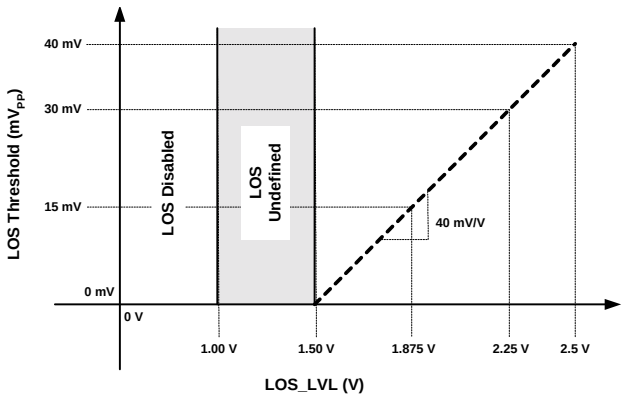


Figure 2. LOS_LVL Mapping

Extended LOS Hysteresis Option

An optional LOS Hysteresis Extension circuit is included on the Si5023-EVB to provide a convenient means of increasing the amount of $\overline{\text{LOS}}$ Alarm hysteresis when testing and evaluating the Si5023 $\overline{\text{LOS}}$ functionality. This simple network will extend the $\overline{\text{LOS}}$ hysteresis to approximately 6 dB, thereby preventing unnecessary switching on $\overline{\text{LOS}}$ for low level DATAIN signals in the range of 20 mV_{PPD}. Hysteresis is defined as the ratio of the $\overline{\text{LOS}}$ deassert level (LOSD) and the $\overline{\text{LOS}}$ assert level (LOSA). The hysteresis in decibels is calculated as 20log(LOSD/LOSA). This circuit is constructed with one CMOS inverter (U2) and two resistors (R12, R13) mounted on the underside of the PCB. If desired, this circuit can be enabled by installing a jumper on JP17 (HYST ENABLE) located near the power entry block.

Data Slicing Level

The slicing level allows optimization of the input cross-over point for systems where the slicing level is not at the amplitude average. The data slicing level can be adjusted from the nominal cross-over point of the data by applying a voltage to the SLICE_LVL pin. SLICE_LVL is controllable through the BNC jack, J11. The SLICE_LVL to the data slicing level is mapped as follows:

$$V_{SLICE} = \frac{V_{SLICE_LVL} - 1.5}{50}$$

If this function is not used, jumper JP6.

Bit-Error-Rate Alarm Threshold

The bit-error-rate of the incoming data can be monitored by the BER_ALM pin. When the bit-error-rate exceeds an externally-set threshold level, BER_ALM is asserted. BER_ALM is brought to a test point located in the upper right-hand corner of the board. The BER_ALM threshold level is set by applying a dc voltage to the BER_LVL pin. BER_LVL is controllable through the BNC jack, J12. Jumper JP7 to disable the BER alarm. Refer to the "BER Detection" section of the Si5022/Si5023 data sheet for threshold level programming. The BER_MON signal (JP14) is reserved for factory testing purposes.

Test Configuration

The three critical jitter tests typically performed on a CDR device are jitter transfer, jitter tolerance, and jitter generation. By connecting the Si5023 Evaluation Board as shown in Figure 3, all three measurements can be easily made.

When applied, REFCLK should be within ±100 PM of the frequency selected from Table 1. RATESEL must be configured to match the desired data rate, and PWRDN/CAL must be unjumpered.

Jitter Tolerance: Referring to Figure 3, this test requires a pattern generator, a clock source (synthesizer signal source), a modulation source, a jitter analyzer, a pattern analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test, the Jitter Analyzer directs the Modulation Source to apply prescribed amounts of jitter to the synthesizer source. This "jitters" the pattern generator timebase which drives the DATAIN ports of the CDR. The Bit-Error-Rate (BER) is monitored on the Pattern Analyzer. The modulation (jitter) frequency and amplitude is recorded when the BER approaches a specified threshold. The Si5023 limiting amplifier can also be examined during this test. Simply lower the amplitude of the incoming data to the minimum value

typically expected at the limiting amplifier inputs (typically 10 mV_{PP} for the Si5023 device).

Jitter Generation: Referring to Figure 3, this test requires a pattern generator, a clock source (synthesizer signal source), a jitter analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test, there is no modulation of the Data Clock; so, the data that is sent to the CDR is jitter free. The Jitter Analyzer measures the RMS and peak-to-peak jitter on the CDR CLKOUT. Thus, any jitter measured is jitter generated by the CDR.

Jitter Transfer: Referring to Figure 3, this test requires a pattern generator, a clock source (synthesizer signal source), a modulation source, a jitter analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test, the Jitter Analyzer modulates the data pattern and data clock reference. The modulated data clock reference is compared with the CLKOUT of the CDR. Jitter on CLKOUT relative to the jitter on the data clock reference is plotted versus modulation frequency at predefined jitter amplitudes.

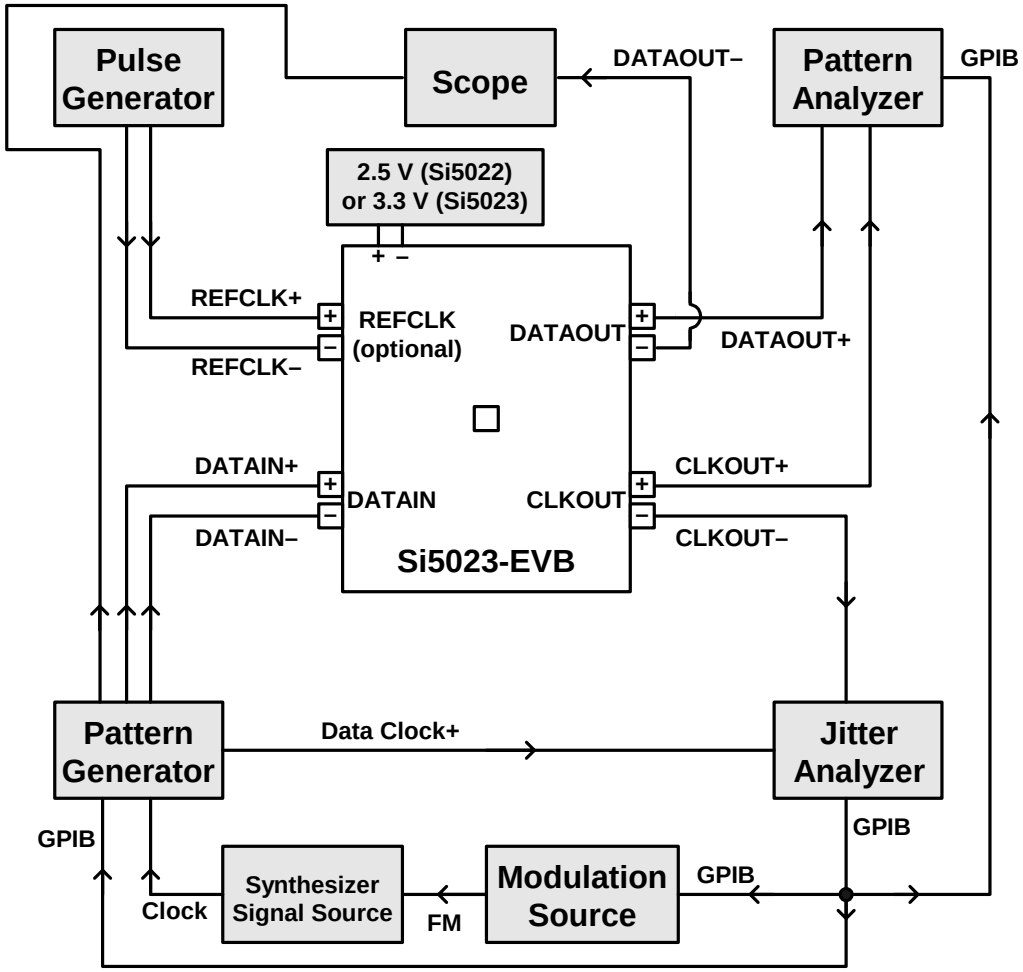


Figure 3. Test Configuration for Jitter Tolerance, Transfer, and Generation

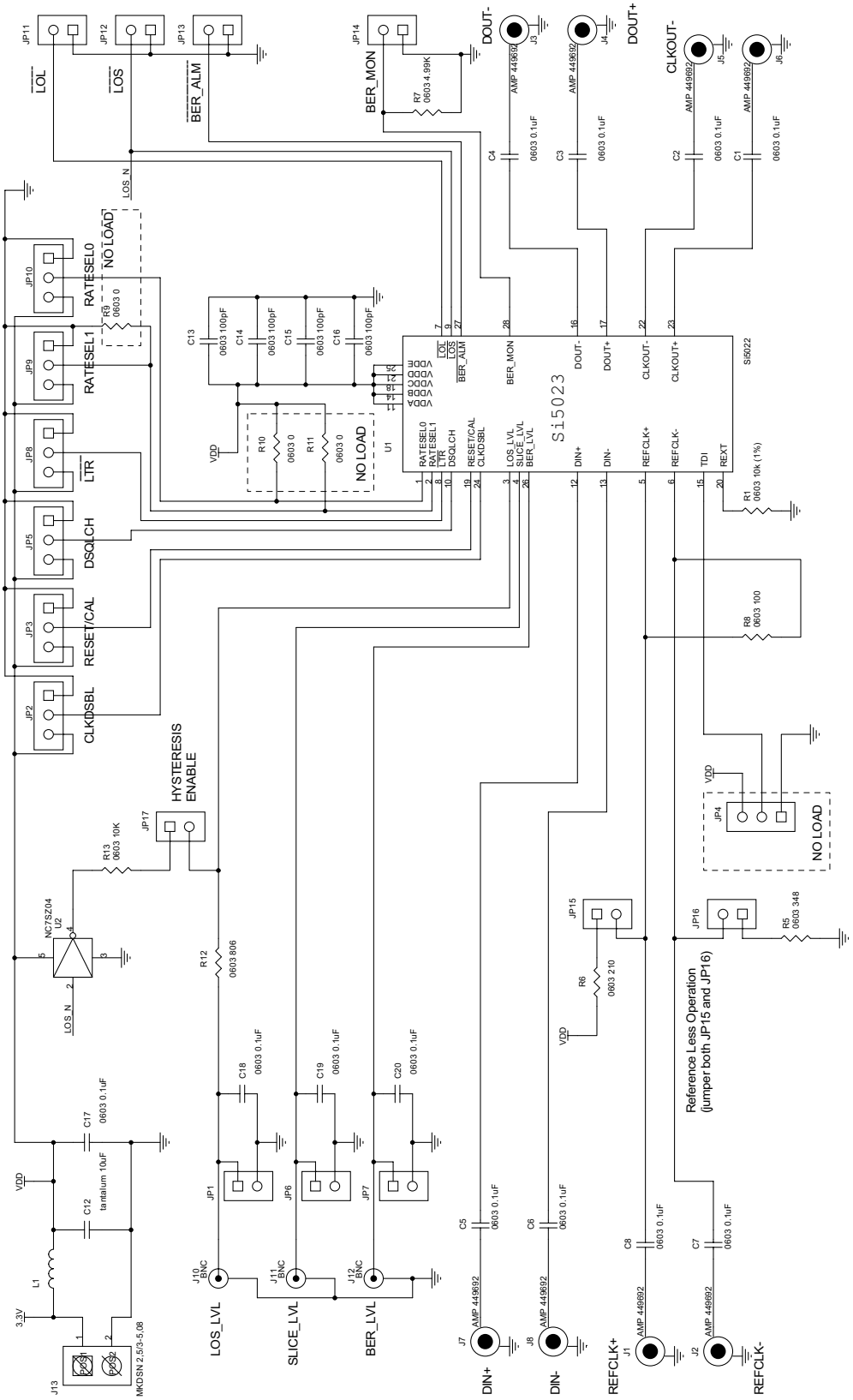


Figure 4. Si5023 Schematic

Bill of Materials

Item	Quantity	Reference	Description	Manufacturer's #	Manufacturer
1	12	C1,C2,C3,C4,C5,C6,	CAP,SM,0.1UF,16V,20%,X7R,0603	C0603X7R160-104KNE	VENKEL
		C7,C8,C17,C18,C19,			
		C20			
2	1	C12	CAP,SM,10UF,10V 10%,TANTALUM,3216	TA010TCM106KAR	VENKEL
3	4	C13,C14,C15,C16	CAP,SM,100PF,50V,10%,C0G,0603	C0603C0G500-101KNE	VENKEL
4	10	JP1,JP6,JP7,JP11,	CONN,HEADER,2X1	2340-6111TN or 2380-6121TN	3M
		JP12,JP13,JP14,			
		JP15,JP16,JP17			
5	6	JP2,JP3,JP5,JP8,	CONN,HEADER,3X1	2340-6111TN or 2380-6121TN	3M
		JP9,JP10			
6	8	J1,J2,J3,J4,J5,J6,	CONN,SMA SIDE MOUNT	901-10003	AMPHENOL
		J7,J8			
7	3	J10,J11,J12	CONN,BNC,VERT	161-9317	MOUSER
8	1	J13	CONN,POWER,2 POSITION	1729018	PHOENIX CONTACT
9	1	L1	FERRITE,SM,600,1206	BLM31A601S	MURATA
10	2	R1,R13	RES,SM,10K,1%,0603	CR0603-16W-1002FT	VENKEL
11	1	R5	RES,SM,348,1%,0603	CR0603-16W-3480FT	Venkel
12	1	R6	RES,SM,210,1%,0603	CR0603-16W-2100FT	VENKEL
13	1	R7	RES,SM,4.99K,1%,0603	CR0603-16W-4991FT	VENKEL
14	1	R8	RES,SM,100,1%,0603	CR0603-16W-1000FT	VENKEL
15	1	R12	RES,SM,806,1%,0603	CR0603-16W-8060FT	VENKEL
16	1	U1	Si5023	Si5023-BM	SILICON LABORATORIES
17	1	U2	IC,SM,7SZ04,SINGLE GATE INVERTER,5 PIN SOT23	NC7SZ04M5X	FAIRCHILD
No Load					
18	3	R9,R10,R11	RES,SM,0,0603	CR0603-16W-000T	VENKEL
19	1	JP4	CONN,HEADER,3X1	2340-6111TN or 2380-6121TN	3M

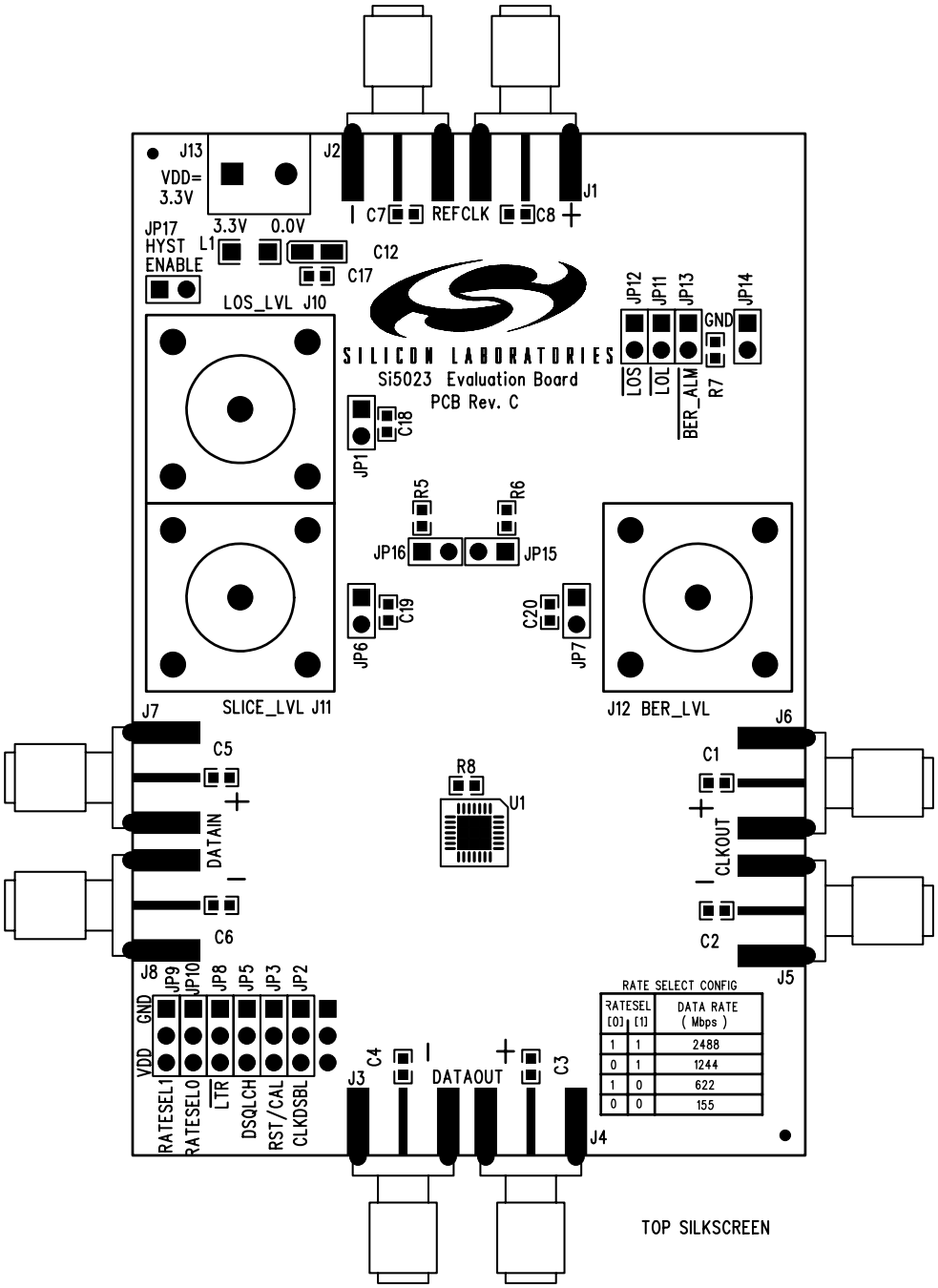


Figure 5. Si5023 Silkscreen

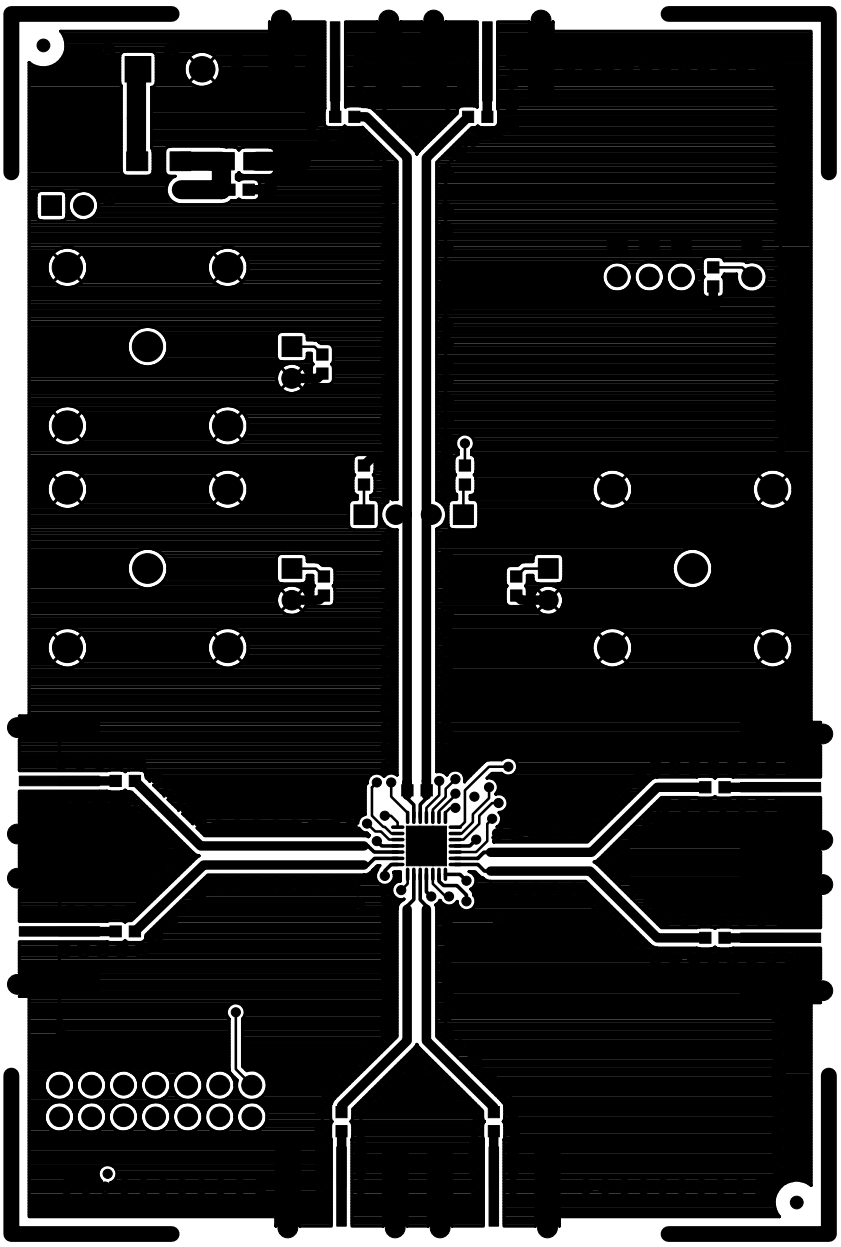


Figure 6. Si5023 Component Side

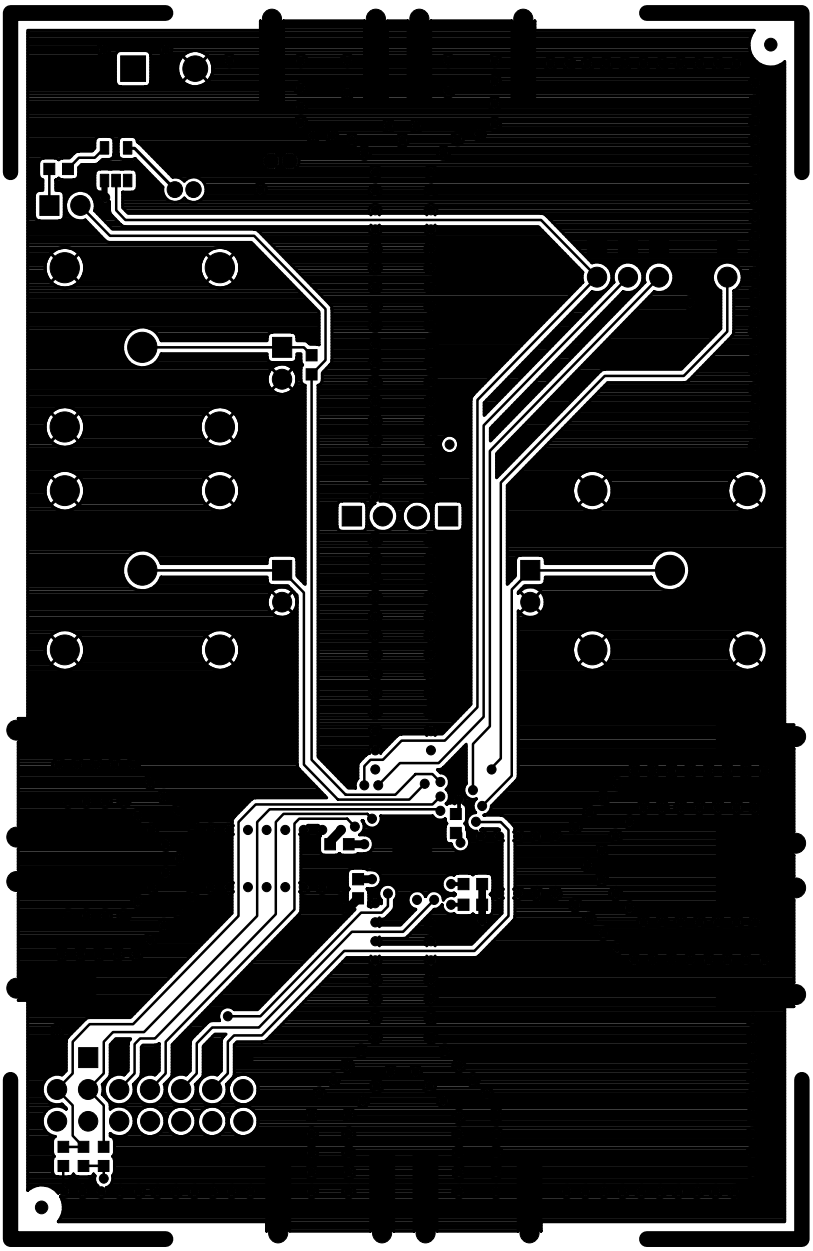


Figure 7. Si5023 Solder Side

Document Change List

Revision 1.0 to Revision 1.1

- Added BER_MON label and 5 kΩ resistor to “Functional Block Diagram” .
- Added "Extended LOS Hysteresis Option," on page 3.
- Revised Figure 4, “Si5023 Schematic,” on page 5 to show extended LOS hysteresis function.
- Revised "Bill of Materials," on page 6 for addition of extended LOS Hysteresis function.

Evaluation Board Assembly Revision History

Assembly Level	PCB	Si5023 Device	Assembly Notes
A-01	A	A	Assemble per BOM rev A-01.
B-01	A	B	Assemble per BOM rev B-01.
B-02	B	B	Assemble per BOM rev B-02.
B-03	C	B	Assemble per BOM rev B-03.

Notes:

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